WHAT IS CLAIMED IS:

1. A memory system, comprising,

a memory bus;

a plurality of memory modules coupled to the memory bus, each memory module including:

a memory array organized for access into a plurality of memory lines;

a code array for storing error codes, including a distinct error code for each of the plurality of memory lines;

access logic for accessing memory lines in the memory array, receiving from the error logic the error detection signal, and initiating a remedial action when the error detection signal indicates that a specified memory line is not consistent with the corresponding error code in the code array;

error logic, coupled to the memory array and code array, for determining whether any specified memory line in the memory array is not consistent with the corresponding error code in the code array and generating a corresponding error detection signal; and

a scheduler, coupled to the access logic, for initiating reading of the memory lines in the memory array in accordance with a memory scrubbing schedule;

wherein each said memory module in the plurality of memory modules concurrently performs memory scrubbing in accordance with the memory scrubbing schedule.

2. The memory system of claim 1, wherein

the scheduler of each memory module in said plurality of memory modules is configured to ensure a scrubbing of at least single bit errors in the memory lines of the memory array during each successive occurrence of a predefined memory scrubbing time period.

3. The memory system of claim 1, wherein

the error logic includes error correction logic for correcting at least a single bit error in the specified memory line when the specified memory line is not consistent with the corresponding error code in the code array; and

each memory module is configured to remove at least single bit errors in the memory lines of the memory array during each successive occurrence of a predefined memory scrubbing time period.

4. A memory system, comprising,

a memory bus;

a plurality of memory modules coupled to the memory bus, each memory module including:

a memory array organized for access into a plurality of memory lines of predefined size, each memory line having a plurality of distinct portions;

a code array for storing error codes, including a distinct error code set for each of the plurality of memory lines, each error code set including a plurality of error codes with a distinct error code for each of the plurality of distinct portions of the associated memory line;

access logic for accessing memory lines in the memory array, receiving from the error logic the error detection signal, and initiating a remedial action when the error detection signal indicates that any portion of a specified memory line is not consistent with the corresponding error code in the code array;

error logic, coupled to the memory array and code array, for determining whether any of the portions of a specified memory line in the memory array is not consistent with the corresponding error code in the code array and generating a corresponding error detection signal; and

a scheduler, coupled to the access logic, for initiating reading of the memory lines in the memory array in accordance with a memory scrubbing schedule;

wherein each said memory module in the plurality of memory modules concurrently performs memory scrubbing in accordance with the memory scrubbing schedule.

5. The memory system of claim 4, wherein

the scheduler of each memory module in said plurality of memory modules is configured to ensure a scrubbing of at least single bit errors in the memory lines of the memory array during each successive occurrence of a predefined memory scrubbing time period.

6. The memory system of claim 4, wherein

the error logic includes error correction logic for correcting at least a single bit error in the specified memory line when any portion of the specified memory line is not consistent with the corresponding error code in the code array; and

each memory module is configured to remove at least single bit errors in the memory lines of the memory array during each successive occurrence of a predefined memory scrubbing time period.

7. A memory module, comprising,

a memory array organized for access into a plurality of memory lines of predefined size, each memory line having a plurality of distinct portions;

a code array for storing error codes, including a distinct error code set for each of the plurality of memory lines, each error code set including a plurality of error codes with a distinct error code for each of the plurality of distinct portions of the associated memory line;

access logic for accessing memory lines in the memory array, receiving from the error logic the error detection signal, and initiating a remedial action when the error detection signal indicates that any portion of a specified memory line is not consistent with the corresponding error code in the code array;

error logic, coupled to the memory array and code array, for determining whether any of the portions of a specified memory line in the memory array is not consistent with the corresponding error code in the code array and generating a corresponding error detection signal; and

a scheduler, coupled to the access logic, for initiating reading of the memory lines in the memory array in accordance with a memory scrubbing schedule.

8. The memory module of claim 7, wherein

the scheduler of said memory module is configured to ensure a scrubbing of at least single bit errors in the memory lines of the memory array during each successive occurrence of a predefined memory scrubbing time period.

9. The memory module of claim 7, wherein

the error logic includes error correction logic for correcting at least a single bit error in the specified memory line when any portion of the specified memory line is not consistent with the corresponding error code in the code array; and

the memory module is configured to remove at least single bit errors in the memory lines of the memory array during each successive occurrence of a predefined memory scrubbing time period.

10. A method of memory scrubbing in a plurality of memory modules coupled to a memory bus, each memory module including a plurality of memory lines organized into a memory array so that each memory line is accessible, for each memory module, the method comprising:

maintaining a code array that includes a distinct error code for each of the plurality of memory lines in the memory array associated with the memory module;

generating an error detection signal that corresponds to a specified memory line in the memory array when any portion of the specified memory line is not consistent with the corresponding error code in the code array;

initiating the reading of the memory lines in the memory array associated with the module in accordance with a memory scrubbing schedule; and

initiating a remedial action when the error detection signal indicates that the specified memory line is not consistent with the corresponding error code in the code array;

wherein each said memory module in the plurality of memory modules concurrently performs memory scrubbing in accordance with the memory scrubbing schedule.

11. The method of claim 10 wherein the memory scrubbing ensures that at least single bit errors in the memory lines of the memory array are scrubbed during each successive occurrence of a predefined memory scrubbing time period.

12. The method of claim 10, wherein said generating step further including the step of correcting at least a single bit error in the specified memory line when any portion of the specified memory line is not consistent with the corresponding error code in the code array; and

each memory module in the plurality of memory modules is configured to remove at least single bit errors in the memory lines of the memory array during each successive occurrence of a predefined memory scrubbing time period.

13. A method of memory scrubbing in a plurality of memory modules coupled to a memory bus, each memory module including a plurality of memory lines of predefined size, each memory line having a plurality of distinct portions, the plurality of memory lines organized into a memory array so that each memory line is accessible, for each memory module, the method comprising:

maintaining a code array that includes a distinct error code set for each of the plurality of memory lines in the memory array associated with the memory module, each error code set including a plurality of error codes with a distinct error code for each of the plurality of distinct portions of the associated memory line;

generating an error detection signal that corresponds to a specified memory line in the memory array when any of the portions of the specified memory line is not consistent with the corresponding error code in the code array;

initiating the reading of the memory lines in the memory array associated with the module in accordance with a memory scrubbing schedule; and

initiating a remedial action when the error detection signal indicates that any portion of the specified memory line is not consistent with the corresponding error code in the code array;

wherein each said memory module in the plurality of memory modules concurrently performs memory scrubbing in accordance with the memory scrubbing schedule.

14. The method of claim 13, wherein the memory scrubbing ensures that at least single bit errors in the memory lines of the memory array are scrubbed during each successive occurrence of a predefined memory scrubbing time period.

15. The memory system of claim 13, the generating step further including the step of correcting at least a single bit error in the specified memory line when any portion of the specified memory line is not consistent with the corresponding error code in the code array; and

each memory module in the plurality of memory modules is configured to remove at least single bit errors in the memory lines of the memory array during each successive occurrence of a predefined memory scrubbing time period.

16. A method of memory scrubbing in a memory module, the memory module including a plurality of memory lines of predefined size, each memory line having a plurality of distinct portions, the plurality of memory lines organized into a memory array so that each memory line is accessible, the method comprising:

maintaining a code array that includes a distinct error code set for each of the plurality of memory lines, each error code set including a plurality of error codes with a distinct error code for each of the plurality of distinct portions of the associated memory line;

generating an error detection signal that corresponds to a specified memory line in the memory array when any of the portions of the specified memory line is not consistent with the corresponding error code in the code array;

initiating the reading to the memory lines in the memory array associated with the module in accordance with a memory scrubbing schedule; and

initiating remedial action when the error detection signal indicates that any portion of the specified memory line is not consistent with the corresponding error code in the code array.

17. The method claim 16, wherein the memory scrubbing ensures that at least single bit errors in the memory lines of the memory array are scrubbed during each successive occurrence of a predefined memory scrubbing time period.

18. The method of claim 16, wherein the generating step further includes the step of correcting at least a single bit error in the specified memory line when any portion of the specified memory line is not consistent with the corresponding error code in the code array; and

the memory module is configured to remove at least single bit errors in the memory lines of the memory array during each successive occurrence of a predefined memory scrubbing time period.